COMMERCIAL MICRO COMPUTER CHIPS FOR INTEGRATED PHASED ARRAY CONTROL

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1. Introduction

Low cost commercial microcomputers, (currently used in many diverse applications, e.g. point-of-sale terminals, desk top computers, check processors, etc.), despite their relatively low computational speed, provide the opportunity for computing beam steering and shaping phase shifts for large phased-array antennas at high beam switching rates through the use of federated multi-computer techniques.

This paper describes microcomputer applications for controlling arrays ranging from a small 100 - element segmented aperture configuration to large 7000 element antennas with beam switching intervals of 600 μs.

With this approach to phased array beam steering the control computing circuits are integrated with the phase shifter drive electronics reducing the former multi-wire interface to a simple parallel computer interface.

2. Statement of the Problem

Modern phased array antennas, because of their inherent beam forming and pointing agility are invariably used in high-speed, time-multiplexed, multi-mode radar applications under the control of a computer. The large number of phase shift elements involved in turn presents a high computing load to set each element with the correct phase shift for a given beam shape and pointing angle. Various methods have been used to date to satisfy the high computing rates required ranging from a single, high-speed, special-purpose beam steering programmer (BSP) to multiple medium and low speed computing units. The latter using serial arithmetic techniques.

From a system design viewpoint the control interface with the antenna is comparable to that of a core-memory stack (Figure 1) with the added disadvantage that the antenna is usually physically separated from the beam steering programmer by wire runs of typically 100 ft.

A further problem which has made the phased array antenna elusive to attempts at standardization is the customary tailoring of each antenna in type, number and configuration of phase shifters to achieve optimum performance for a specific radar application.

In the area of control however, two recent studies have identified the micro-computer as a key to making the antenna complete and self sufficient, with the interface of a conventional computer peripheral device, requiring only beam pointing azimuth and elevation angles and operating radar wavelength as digital inputs. Further, variations in antenna configurations and performance can be tracked by re-programming the co-located micro computers. High switching speeds are achieved through the parallelism of computer modules, a one-time luxury which can now be realized at considerably lower cost due to the high-volume production runs of LSI microcomputer chips.

3. Performance Requirements

Before discussing the two specific applications of microcomputers to phased array antenna control recently studied, the basic performance requirements will be briefly reviewed.

As stated earlier in this paper, the forming and pointing of the beam requires the computation of phase shift values for each and every element in the array.

For a symmetrical array, the phase shift control equation is typically of the following form:

$$\Psi_{M,N} = M\Delta_M + N\Delta_N + C(M,N,r) + S_n(M,N;\emptyset) \quad \text{Mod } 2\pi$$

Where:

- M & N - column and row numbers respectively
- $\Psi_{M,N}$ - phase setting for an element at location M,N modulo 2π.
- Δ_M, Δ_N - differential phase shift between adjacent columns and rows respectively
- C - collimation term
- r - index of refraction in the feed guide
- S_n - beam shaping term
- $\emptyset$ - antenna roll angle.

Beam polarization is invariably a static or quasistatic phase term applied to all phase shifters from a common source and is therefore excluded from the above equation.

In cases where collimation and shaping for beams other than pencil shape are not required, the equation reduces to the $M\Delta_M + N\Delta_N$ steering phase component. Δ_M and Δ_N being a function of pointing angle and operating wavelength, are computed once per beam position and used for

incrementally computing the absolute phase value for all elements in a given column and row respectively, modulo 2π.

Real time inputs to the BSP (azimuth and elevation direction sizes, operating wavelength and roll angle) usually do not exceed 12 bits in magnitude, and computations within the BSP similarly do not require word lengths in excess of the latter. The final phase shift value for a given element after round-off is typically 3 to 4 bits magnitude, and this is either used to control PIN diode phase shifters, in straight binary form or, alternatively is converted to a proportional pulse width to drive the phasing coil of a ferrite shifter after initial resetting.

Beam switching intervals typically range from 10-20 μs up to 1 ms.

Array sizes range from approximately 500 to 12,000 elements.

The composite computing load can therefore be extremely high in the 12,000 element 10-20 μs situation but this is normally overcome by taking advantage of array quadrant symmetry, separation of row and column phase components for summation at the element, and zoning for collimation correction instead of discrete element compensation.

4. Available Microcomputers

Table 1 shows a representative listing of microcomputers currently on the market. The first two being initially developed for sophisticated calculator applications. The first having the input-output ports incorporated in the memory modules whereas the others utilize standard LSI read/write and read-only memory circuits. The recent announcement of N-channel MOS microcomputers holds the greatest promise for application in military environments.

5. Microcomputer Mechanizations

The two antenna systems considered during the recent studies are representative of the two extremes in the spectrum of antenna configurations, respectively. One antenna was a 100-element matrix sector of a broadband segmented aperture array, while the other was a 6,960-element array with isosceles triangular spacing of elements. Both arrays employed PIN diode phase shifters, although it can be shown that the micro-computer approach offers similar advantages in ferrite element control.

5.1 Broadband Segmented Aperture Array

This case involved the control of a 10x10 matrix as a modular subarray for use in larger antennas by replication of the basic 100-element module.

Figure 2 shows the basic system configuration with the microcomputer co-located on the array to provide the computation of phase shift and polarization settings as 8-bit control words to each phase shift element, and the common control interface for three different command sources: manual by element, manual by beam position and automatic under the control of the radar control minicomputer. The similarity between a calculator keyboard switch matrix and the array matrix is readily apparent and this in turn, provides the key to readily interfacing the array with a microcomputer, since the latter devices normally interface with such calculator components. Similar advantages can be realized in the design of the manual control units through the use of other standard calculator components such as light emitting diode (LED) or liquid crystal displays and compatible micro-computer interface hardware. Figure 3 shows a 4-bit micro-computer set configured to drive the 100 element array. Rough order of magnitude cost for the LSI circuits would be $100.00 for large quantities.

5.2 Large, High-Speed, Array Control

The size of the antenna considered was a 6,960-element array organized in 163 rows and 107 columns with quadrant symmetry. Beam switching intervals to be considered were 250,500 and 1000 μs respectively. The control equation contained only pointing and collimation terms (i.e. pencil beam shape). Row and column control was acceptable with zoning in groups of up to 16 elements for collimation correction. The respective row and column phase equations given were as follows:

$$\Psi_N = N\frac{2\pi dy}{\lambda}\sin\theta + \frac{b\pi N^2 dy^2}{\lambda F}$$

$$\Psi_M = M\frac{2\pi dx}{\lambda}\sin\psi + \frac{a\pi M^2 dx^2}{\lambda F}$$

Where,

Ψ_N = Row phase component for all elements in row N

Ψ_M = Column phase component for all elements in column M

dy = Spacing between each row

dx = Spacing between each column

λ = Wavelength

θ = Beam elevation angle with respect to antenna axis

ψ = Beam azimuth angle with respect to antenna axis

F = Focal length of the array

a,b = Collimation zone correction terms

TABLE 1. MICRO COMPUTER CHARACTERISTICS

Manufacturer and Computer Type	Word Length	Register Register Add (μs)	Clock Freq. kHz	Instruction Set	Basic Computer (Qty) ICs	Basic Computer Cost $ 100-999	Expanded Memory	Device Technology & Packaging
'A' Type 1	4	10.8 (4+4)	750.0	45 Add, Sub	(1) CPU: 16x4 Registers (1) RAM: 80x4 (1) ROM: 256x8	30.00 15.00 15.00	ROM 4Kx8 RAM 1.2K x4	P-MOS Si Gate CPU: 16 PIN C DIP RAM: 16 PIN P DIP ROM: 16 PIN P DIP
'A' Type 2	8	12.5 (8+8)	800.0	48 Add, Sub	(1) CPU: 7x8 Registers *(8) RAM: 256x8 (1) ROM: 256x8	90.00 16.50	16Kx8 RAM/ROM	P-MOS Si Gate CPU: 18 PIN C DIP RAM: 16 PIN DIP ROM: 24 PIN DIP
'A' Type 3	8	2.0 (8+8)	2 MHz	74 Add, Sub	(1) CPU: 7x8 *(8) RAM: 1024x8 (1) ROM: 2048x8	100.00 191.20 48.00	65Kx8 RAM/ROM	N-MOS Si Gate CPU: 40 PIN DIP RAM: 16 PIN DIP ROM: PIN DIP
'B'	4	62.5	400 kHz	95 Add, Sub	(1) ALU: 25x4 Registers (1) Timing: (1) ROM: 256x12 (1) RAM: 75x4		ROM 6Kx12 RAM 175x4	P-MOS Si Gate ALU: 18 PIN DIP Timing: 24 PIN DIP ROM: 16 PIN DIP RAM: 16 PIN DIP
'C'	16	4.9	3 MHz	42 Add, Sub	62 ICs on 8 1/2" x 11" PCB 4 x 4 Bit ALUs 4 GP Registers	495.00 without ROMs. + 50.00 for 4 2K PROMS	65Kx16	P-MOS & T^2L Complete 16-Bit Computer on 8 1/2"x11" PCB 256 x 16 RAM 512 x 16 ROM

*RAM is optional for small data base.

5.2.1 Requirements Analysis. From the above requirements it becomes necessary to compute only the beam pointing commands for one quadrant of the array and by symmentry to add the collimation term to the true/complement values of the steering terms to obtain the phase shift settings for the remaining three quadrants.

The total computing load can be broken down as follows:

Computation	Per Beam
$\Delta_N = \frac{2\pi dy}{\lambda} \sin\theta$	1
$\Delta_M = \frac{2\pi dx}{\lambda} \sin\psi$	1
$N\Delta_N$	82
$M\Delta_M$	54
$\overline{N\Delta}_N$	82
$\overline{M\Delta}_M$	54
$C_N = \frac{b\pi N^2\, dy^2}{\lambda F}$	82
$C_M = \frac{a\pi M^2\, dx^2}{\lambda F}$	54

Computation	Per Beam	
$\Psi_N = N\Delta_N + C_N$	82	
$\Psi_{-N} = \overline{N\Delta}_N + C_N$	82	
$\Psi_M = M\Delta_M + C_N$	54	
$\Psi_{-M} = \overline{M\Delta}_M + C_N$	54	
$(Q_1)\ \Psi_N + \Psi_M$	1740	
$(Q_2)\ \Psi_N + \Psi_{-M}$	1740	Simultaneous at all elements
$(Q_3)\ \Psi_{-N} + \Psi_{-M}$	1740	
$(Q_4)\ \Psi_{-N} + \Psi_M$	1740	

The corresponding computer flow charts to perform the above operations on an 8-bit, 2 μs, microcomputer (one per row pair and one per column pair) are shown in Figure 4. Total running time is estimated at approximately 100 μs for one pass plus an additional 12 μs for each subsequent iteration through the collimation/output path for zone correction. Table 2 summarizes the large and medium scale integrated circuit (IC) counts required for each of the three beam switching intervals together with the corresponding cost estimates. The non-recurring design cost would remain virtually constant for all three cases since the basic computer set would be replicated. Figure 5 shows the resulting system configuration with the microcomputer ICs packaged on the array.

6. Conclusion

The status of current methods for controlling phased array antenna beam shapes and positions has been briefly reviewed in the light of the burgeoning microcomputer technology and, from the two examples considered, the microcomputer and its associated interface circuits offers a low-cost solution to the design of antennas as fully integrated components for direct control by the radar subsystem computer. Further, the flexibility required to meet the wide variety of radar applications can be accommodated in simple microcomputer software at low operating speeds, in contrast to the customary design of new special-purpose computer hardware.

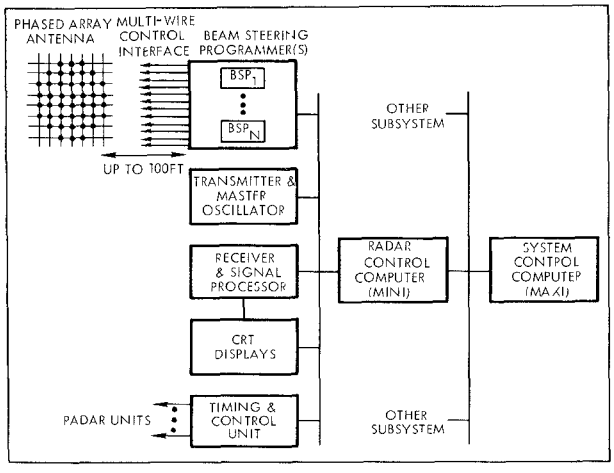

Figure 1. Control & Interface of Phased Array Antenna in typical present day multi-mode Radar System.

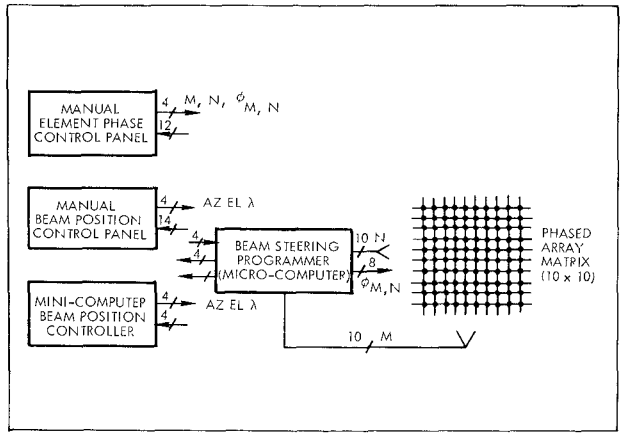

Figure 2. Microcomputer Control of 10x10 Array Matrix, System Block Diagram.

TABLE 2. LARGE, HIGH-SPEED, ARRAY CONTROL MICROCOMPUTER HARDWARE ESTIMATES

Beam Switching Interval	Design Approach	Number of ICs	Material Cost (K$)
250 μs min.	Microcomputer per row pair (82 ea.) and column pair (54 ea.)	1,090	32.0
500 μs min.	Microcomputer per 4 rows (41 ea.) and per 4 columns (27 ea.)	546	16.0
1000 μs min.	Microcomputer per 8 rows (20 ea.) and per 8 columns (13 ea.)	266	80